First Named Inventor: Frankie F. Roohparvar Title: SYNCHRONOUS FLASH MEMORY WITH TEST CODE INPUT Atty Docket No: 400.017US01 Filing Date: April 9, 2001 Serial No: 09/829,136 JUN 0 1 2004 **→** CAS# **₩** RAS# MØQ ★ 1/3 **→** CKE #SO ★ ¥ RP# DQ0-DQ15 200 Processor A0-A11 BA0,BA1 DOML, 힝 128 Data Input Register Data Output Register Status Reg. BANK2 / BANK 1 / BANK 0 Memory Array (4,096 x 256 x 16) I/O Gating DOM Mask Logic Read Data Latch Write Drivers Sense Amplifiers 90 High Voltage Switch/Pump Address Latch & Decoder BANK 0 ROW-Column-Address Counter/ Latch Bank Control Logic ROW-Address Mux State Machine 132 130 148 147 Command Execution Logic Mode Register NVMode Register 12 Address Register 8 96 Command Decode Detect



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Vcc DQ0 VccQ	HHH	1* 2 3			54 53 52	888	Vss DQ15 VssQ	
DQ1	Щ	4			51		DQ14	
DQ2 VssQ		5 6	150		50 49	片	DQ13 VccQ	
	H	7	<u>150</u>		48	H	DQ12	
		8			47	Б	DQ11	
	Щ	9			46		VssQ	
DQ5	四	10			45		DQ10	
DQ6 VssQ	出	11 12			44 43	出	DQ9 VccQ	
DQ7	H	13			42	H	DQ8	
Vcc		14			41		Vss_	
DQML	Ш	15			40		RP#	—152
• • • • • •	Щ	16			39		DQMF	1
CAS#		17			38	田	CLK	
		18 19			37 36	H	CKE VccP	—154
	뀌	20			35	Ħ	A11	
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, , ,	田	23			32	口	A7	
	四	24			31		A6	
A2 A3		25			30		A5 A4	
	띪	26 27			29 28	片	Vss	
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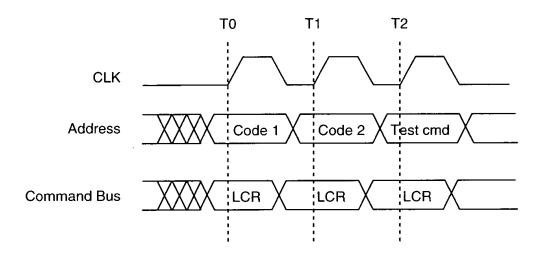


Fig. 3